(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 967 643 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication
29.12.1999 Bulletin 1999/52

(51) Int Cl 6 H01L 21/8242

(21) Application number 99304729.9

(22) Date of filing: 17.06.1999

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 22.06.1998 US 102471

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(54) Low-resistance salicide fill for trench capacitors

(57) Trench capacitors are fabricated utilizing a method which results in a refractory metal salicide as a component of the trench electrode in a lower region of the trench. The salicide-containing trench electrode exhibits reduced series resistance compared to conventional trench electrodes of similar dimensions, thereby enabling reduced ground rule memory cell leats and/or reduced cell access time. The trench capacitors of the invention are especially useful as components of DRAM memory cells.

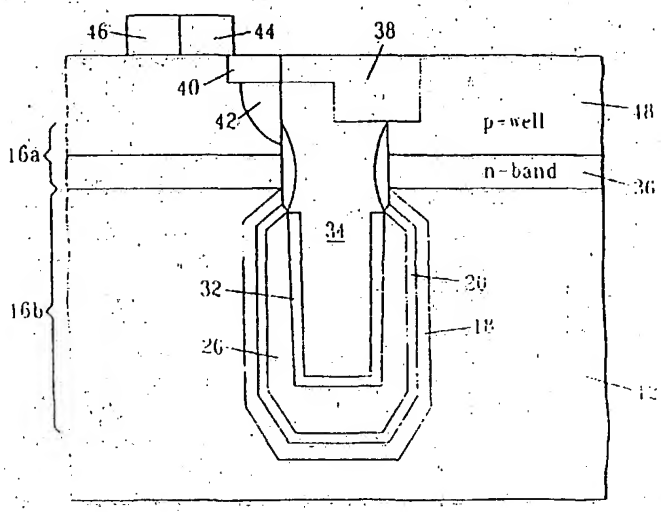

FIG. 2

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Description

[0001] The present invention relates to the manufacture and design of trench capacitors for integrated circuit devices, especially capacitors for use in dynamic random access memory (DRAM) cells and advanced memory devices containing the same

[0002] Generally a semiconductor memory device such as a dynamic random access memory (DRAM) cell comprises a plurality of memory cells which are used to store large quantities of information. Each memory cell typically includes a capacitor for storing electric charge and a field effect transistor (FET) for opening and closing charge and discharge passages of the capacitor. The number of cells (and corresponding bits of memory capacity) of DRAM integrated circuit chips has been increasing by approximately 4X every three years; this has been achieved by reducing memory cell size. Unfortunately, the smaller cell size also results in less area to fabricate the capacitor.

[0003] Moreover, as DRAM cell dimensions are scaled down with each successive generation, the cross-sectional area of the deep trench storage capacitor diminishes inversely with the square of the ground rule, while the trench depth has remained approximately constant. This change in trench geometry results in a large increase in the series resistance contributed by the polysilicon electrode contained in the deep trench. The increased resistance in turn may adversely limit the speed at which the corresponding memory cell can be accessed.

[0004] One approach to decrease the series resistance of DRAM trench capacitors is to increase the doping concentration of the deep trench polysilicon. This approach however only provides a marginal reduction in series resistance and thus has limited applicability in fabricating DRAM cells of decreased dimension.

[0005] Thus, there is a continued need for new manufacturing processes and/or designs which more effectively address the problem of series resistance in the context of trench capacitors and devices incorporating such capacitors (e.g., DRAM chips).

[0006] The present invention provides trench capacitor structures and methods of fabricating trench capacitors wherein the distributed series resistance of the deep trench electrode is substantially reduced for a given trench geometry.

[0007] The present invention provides trench capacitor structures and methods of fabricating trench capacitors wherein the series capacitance of the deep trench electrode is substantially increased for a given trench geometry.

[0008] The present invention further provides a trench capacitor structure which can be used conventional DRAM and in advanced memory cell devices.

[0009] In a first aspect, the invention accordingly provides a method of fabricating a trench capacitor structure in a semiconductor substrate, said method comprising (a) providing a semiconductor substrate having (i) a trench therein, said trench having a narrow upper region and a broad lower region (ii) an electrode in said substrate about said broad lower region, and (iii) a conformal node dielectric lining said trench at said electrode (b) filling said trench with a layer of polysilicon leaving a void in said broad lower region of said trench, (c) planarizing the structure resulting from step (b), (d) removing the layer of polysilicon in said narrow upper region of said trench, said void in said broad lower region of said trench being exposed; (e) forming a conformal refractory metal layer in said narrow upper region and said broad lower region; (f) annealing said structure to form a refractory metal salicide layer in said broad lower region of said trench structure; (g) removing said conformal refractory metal layer from said narrow upper region of said trench; (h) filling said trench structure with polysilicon; and (i) planarizing the structure resulting from step (h).

[0010] Step (e) is preferably conducted using a selective reaction which is capable of converting the refractory metal formed in the broad lower region of said trench to a refractory metal salicide having low-resistance.

[0011] Preferably, in the first aspect, said semiconductor substrate is Si. Said electrode is preferably an out-diffused buried plate. Preferably also a collar oxide is provided about the upper region of said trench prior to step (b). It is also preferred that step (b) is carried out by low pressure chemical vapour deposition. Said void is further preferably completely covered by said polysilicon deposited in step (b).

[0012] Preferably, in the first aspect, step (c) is carried out by chemical mechanical polishing or etching. It is preferred to have the method of the first aspect in which said removal step (d) comprises etching said polysilicon by anisotropy etching, isotropic etching or a combination thereof. Preferably, said etching is performed by ion enhanced etching, ion induced etching, plasma etching, reactive ion etching, reactive ion-beam etching or microwave plasma etching.

[0013] Preferably, in the method of the first aspect, step (d) is carried out by plasma etching utilizing a halogen as a reactive plasma gas. Also preferably, in the method of the first aspect, said polysilicon is completely removed from said narrow upper region in step (d). The method of the first aspect preferably has step (e) carried out by chemical vapour deposition, sputtering, electroplating or electroless-plating.

[0014] It is preferred in the method of first aspect to have said refractory metal selected from the group consisting of Ta, W, Co, Ti and Mo. It is further preferred in the first aspect that said annealing be conducted in the presence of a non-oxidizing atmosphere. Preferably, also, said annealing is carried out at a temperature of about 600° to 1000°C for about 5 seconds to 1 hour; and preferably, said annealing is carried out at a temperature of about 700° to 800°C for about 10 to 60 sec-

onds

[0015] It is preferred in the method of the first aspect that said refractory metal salicide have a resistivity of about 15 to 150 μohm-cm, and further preferred that said refractory metal salicide have a resistivity of about 15 to 25 μohm-cm

[0016] It is preferred in the method of the first aspect that said refractory metal be removed in step (g) by wet chemical etching with a chemical etchant selected from the group consisting of H_2O_2, HCl, HNO_3, acetic acid, chromic acid, phosphoric acid, sulfuric acid, ammonium hydroxide and mixtures thereof

[0017] In a second aspect, the present invention provides a capacitor structure in a semiconductor substrate, said capacitor structure comprising (i) a trench having a narrow upper region and a broad lower region, (ii) an electrode in said substrate about said broad lower region, (iii) a conformal node dielectric lining said trench at said electrode, and (iv) a second electrode in said trench, said second electrode in said broad lower region comprising a first layer of polysilicon over said node dielectric, a refractory metal salicide layer over said first polysilicon layer and a second polysilicon layer over said salicide.

[0018] The second aspect of the present invention relates to a trench capacitor structure having a salicide present in the trench. The capacitor structure of the present invention is preferably useful as a storage capacitor in a DRAM memory cell. The capacitor structure of the invention preferably comprises a storage trench having a narrow upper region and a broad lower region, wherein the broad lower region comprises an outer layer of polysilicon over which is formed a refractory metal salicide layer and a polysilicon inner layer. The storage trench is preferably bottle-shaped.

[0019] It is preferred in the capacitor structure of the second aspect that said semiconductor substrate be Si. Also preferred is that the capacitor structure of the second aspect comprise a collar oxide about said narrow upper trench region.

[0020] Preferably, said refractory metal salicide contains a refractory metal selected from the group consisting of Ta, W, Co, Ti and Mo.

[0021] Preferably, also, the capacitor structure of the second aspect comprises said refractory metal salicide with a resistivity of about 15 to 150 μohm-cm, and further preferably said refractory metal salicide has a resistivity of about 15 to 25 μohm-cm.

[0022] In a third aspect, the present invention provides a memory cell device comprising the trench capacitor structure of the second aspect.

[0023] The third aspect of the present invention is directed to advanced memory cell devices which contain at least the DRAM cell capacitor structure of the present invention therein as one of its components.

[0024] In a fourth aspect, the present invention provides a capacitor structure in a semiconductor substrate, said capacitor structure comprising (i) a trench having a upper region and a lower region, (ii) an electrode in said substrate about said lower region, (iii) a conformal node dielectric lining said trench at said electrode, and (iv) a second electrode in said trench, said second electrode in said lower region comprising a first layer of polysilicon over said node dielectric, a refractory metal salicide layer over said first polysilicon layer and a second polysilicon layer over said salicide.

[0025] A preferred embodiment of the present invention will now be described by way of example with reference to the accompanying drawings, in which:

[0026] Figs. 1(a)-(g) are cross-sectional views of a refractory metal salicide-containing bottle-shaped storage trench capacitor structure which is formed from the processing steps of an embodiment of the present invention.

[0027] Fig. 2 is a cross-sectional view of an advanced memory cell device which can be fabricated from the capacitor structure shown in Fig. 1(g).

[0028] Figs. 1(a)-(g) show various processing steps that may be employed in the present embodiment for fabricating a DRAM cell capacitor structure of the invention. Specifically, Fig. 1(a) shows a cross-sectional view of an initial bottle-shaped trench structure 10 that is employed in step (a) of the present embodiment. The bottle-shaped trench structure shown in Fig. 1(a) comprises a semiconductor substrate 12 preferably having a lightly doped epitaxial region 14 and one or more pad dielectric layers 24. The pad dielectric layer (typically a silicon nitride) acts as a protective layer during the etching process used to form trench 16. Trench 16 preferably has a narrow upper region 16a and a broad lower region 16b. In some instances, it may be desirable to form a thin oxide layer (not shown) between semiconductor substrate 12 and pad dielectric 24.

[0029] Semiconductor substrate 12 may be formed from any conventional semiconducting material including, but not limited to: Si, Ge, GaP, InAs, InP, SiGe, GaAs or other III/V compounds. Of these semiconducting materials, it is highly preferred that semiconductor substrate 12 be composed of Si.

[0030] At broad lower trench region 16b, there is shown a buried plate out-diffused region 18 and node dielectric layer 20. Narrow upper region 16a preferably contains an oxide collar 22 which may be formed by local oxidation of silicon (LOCOS) or other technique.

[0031] The initial bottle-shaped structure shown in Fig. 1(a) is fabricated using conventional techniques that are well known to those skilled in the art. For example, the bottle-shaped structure of Fig. 1(a) can be fabricated using the processes disclosed in U.S. Patent Nos. 4,649,625 to Lu, 5,658,816 to Rajeevakumar and 5,692,281 to Rajeevakumar. The buried plate may be formed by any conventional technique of diffusing the appropriate conductivity type dopant through the trench wall. See for example the technique disclosed in U.S. Patent 5,395,786.

[0032] In accordance with the present embodiment,

the structure shown in Fig. 1(a), particularly narrow upper trench region 16a and broad lower trench region 16b, is filled with a layer of polysilicon 26 under deposition conditions that are sufficient to form void 28 in broad lower trench region 16b. The polysilicon layer 26 is then planarized to give the structure shown in Fig. 1(b).

[0033] The polysilicon and void which are shown in Fig. 1(b) are formed in the lower trench region of the bottle-shaped trench capacitor structure utilizing conventional deposition techniques such as chemical vapour deposition (CVD) or low pressure chemical vapour deposition (LPCVD). Of these deposition techniques, LPCVD is highly preferred in the present embodiment for forming polysilicon layer 26 and void 28. The deposition conditions employed in depositing polysilicon layer 26 and forming void 28 may vary depending upon the exact technique used and the trench geometry. In most instances, the deposition conditions used would be those conventionally used for polysilicon fill. The void would result from the closing off of narrow region 16a by polysilicon deposition on the trench wall. If the deposition conditions selected do not result in formation of the desired void, a void may be formed or expanded using an etching technique as described in U.S. Patent 5,692,281 after the polysilicon planarization.

[0034] The polysilicon may be planarized utilizing conventional planarization techniques. For example, the planarization process may be carried out utilizing chemical mechanical polishing (CMP) or etching.

[0035] After planarization, the polysilicon fill 26 is preferably recessed as shown in Fig. 1(c) whereby polysilicon layer 26 in the narrow upper trench region 16a is selectively removed to expose void 28 in the broad lower region 16b. The recessing step may be carried out utilizing any conventional anisotropy or isotropic etching process. Alternatively, a combination of anisotropy and isotropic etching techniques may be used to recess polysilicon 26. Examples of suitable etching techniques include ion enhanced etching, ion induced etching, plasma etching, reactive ion etching, reactive ion-beam etching, microwave plasma etching, chemical etching or other like etching techniques. The recessing is preferably performed by a plasma etching process utilizing a halogen such as chlorine or fluorine as the reactive plasma gas. Assuming the previously formed void 28 is of a sufficient size, the recessing process employed preferably does not substantially remove polysilicon from the broad lower region 16b of the trench. As noted above, it may be desired to form or increase the void size as part of or subsequent to the recessing step.

[0036] After the recessing, a conformal refractory metal layer 30 is deposited as shown in Fig. 1(d). The refractory metal layer may be formed utilizing any conventional deposition process which is capable of forming a conformal layer. Examples of suitable deposition techniques are CVD, sputtering, electroplating, electroless-plating or other like deposition processes. The refractory metal layer 30 is preferably formed by CVD.

[0037] Various refractory metals may be used to form layer 30. Examples of suitable refractory metals are Ti, Ta, W, Co, Mo or other like refractory metals that are capable of forming a metal salicide when annealed in the presence of a silicon-containing material. Thus, for example if a layer of Ti is formed the annealing conditions discussed below are capable of converting Ti to TiSix (preferably $TiSi_2$).

[0038] After deposition of refractory metal layer 30, a refractory metal salicide layer 32 is formed in broad lower trench region 16b as illustrated in Fig. 1(e) by annealing which causes salicide formation at the refractory metal - polysilicon interface in region 16b. It is highly preferred that no refractory metal salicide is formed in the narrow upper trench region 16a. Formation of salicide region 16a is prevented by the collar oxide 22 and by removal of polysilicon from region 16a during the recessing step.

[0039] The annealing step employed in the present embodiment is preferably conducted in the presence of a non-oxidizing ambient such as helium, nitrogen, argon or mixtures thereof. The annealing step may be carried out at atmospheric pressure or under a suitable vacuum. The annealing is preferably carried out at a temperature of about 600° to 1000°C for a time period of about 5 seconds to 1 hour. Shorter annealing times are typically employed with higher annealing temperatures, whereas longer annealing times are typically employed with lower annealing temperatures. More preferably, the annealing step is carried out at a temperature of about 700° to 800°C for a time period of about 10 seconds to 60 seconds. The annealing step can be carried out at a set temperature or it can be ramped up to a desired temperature utilizing various ramp and soak cycles.

[0040] The refractory metal salicide formed by the annealing step of the present embodiment preferably has a measured resistivity of about 15 to 150 µohm-cm. More preferably, the resistivity of the refractory metal salicide formed in the annealing step is about 15 to 25 µohm-cm.

[0041] After formation of the desired refractory metal salicide layer 32 in the broad lower region 16b of the trench structure, the remaining refractory metal layer 30 in upper region 16a is removed. The resulting structure is illustrated in Fig. 1(f). Preferably, a chemical wet etch process that is highly selective in etching refractory metal is used to remove remaining layer 30. Any chemical etchant that is capable of removing the refractory metal from the upper trench region of the capacitor structure can be employed. Illustrative examples of suitable chemical etchants are H_2O_2, HCl, HNO_3, acetic acid, chromic acid, phosphoric acid, sulfuric acid, ammonium hydroxide or other like chemical etchants. Mixtures of these chemical etchants with each other or with water may also be used. H_2O_2 is a preferred chemical etchant.

[0042] After removal of the refractory metal 30 from the upper region 16a of the trench structure, the trench

is then filled with additional polysilicon 34 utilizing any of the above mentioned deposition processes used in forming polysilicon layer 26. The capacitor structure is then planarized using any of the above planarization techniques or plasma etching to give the capacitor structure shown in Fig 1(g)

[0043] The capacitor structure containing refractory salicide layer 32 in the broad lower region of the trench has substantially reduced series resistance than comparable structures that do not contain such a metal salicide layer therein. Typically, this is capable of reducing the series resistance caused by the deep trench polysilicon as much as 100x for a given trench geometry/ground rule. Alternatively, the method may be used to create capacitor structures with even smaller ground rule which have series resistance similar to wider capacitor structures.

[0044] The capacitor structures may be used in DRAM memory cells such as the one shown in Fig. 2 or in other integrated circuit devices Specifically, memory cell in Fig. 2 comprises the capacitor structure shown in Fig. 1(g) as well as n-band region 36, p-well 48, shallow trench isolation region 38. buried strap region 42, array implant region 40, gate conductor region 44 and array conductor region 46.

[0045] The memory cell device shown in Fig. 2 may be fabricated utilizing the present method in combination with other manufacturing steps to form shallow trench isolation, gate conductor regions and other memory cell components, which other manufacturing steps are well known to those. skilled in the art. The formation of n-band regions is discussed in European Published Patent Application 822599, published Feb. 4, 1998. Examples of those manufacturing steps are disclosed in the above mentioned patent document or are otherwise known to those skilled in the art

[0046] In addition to memory cells and the manufacture thereof, the capacitor structures and manufacturing techniques may also be useful in conjunction with other integrated device structures anc device manufacturing techniques.

[0047] It will be readily seen by those of ordinary skill in the related art that the invention is not limited to the specific structures illustrated in the drawings. While the drawings illustrate a bottle-shaped trench the invention may be practised using trenches of other shapes and employing alternative void-forming techniques as discussed above. It should also be understood that the invention is not limited to use of any specific dopant type provided that the dopant types selected for the various components are consistent with the intended electrical operation of the device

Claims

1. A method of fabricating a trench capacitor structure in a semiconductor substrate said method comprising

(a) providing a semiconductor substrate having (i) a trench therein. said trench having a narrow upper region and a broad lower region. (ii) an electrode in said substrate about said broad lower region, and (iii) a conformal node dielectric lining said trench at said electrode

(b) filling said trench with a layer of polysilicon leaving a void in said broad lower region of said trench;

(c) planarizing the structure resulting from step (b);

(d) removing the layer of polysilicon in said narrow upper region of said trench, said void in said broad lower region of said trench being exposed;

(e) forming a conformal refractory metal layer in said narrow upper region and said broad lower region;

(f) annealing said structure to form a refractory metal salicide layer in said broad lower region of said trench structure;

(g) removing said conformal refractory metal layer from said narrow upper region of said trench;

(h) filling said trench structure with polysilicon; and

(i) planarizing the structure resulting from step (h).

2. The method of Claim 1 wherein said electrode is an out-diffused buried plate.

3. The method of Claim 1 wherein a collar oxide is provided about the upper region of said trench prior to step (b).

4. The method of Claim 1 wherein said removal step (d) comprises etching performed by ion enhanced etching, ion induced etching, plasma etching reactive ion etching, reactive ion-beam etching or microwave plasma etching.

5. The method of Claim 1 wherein step (e) is carried out by chemical vapour deposition. sputtering electroplating or electroless-plating.

6. The method of Claim 1 wherein said annealing is carried out at a temperature of about 600° to

1000°C for about 5 seconds to 1 hour

7. A capacitor structure in a semiconductor substrate said capacitor structure comprising (i) a trench having a narrow upper region and a broad lower region, (ii) an electrode in said substrate about said broad lower region, (iii) a conformal node dielectric lining said trench at said electrode, and (iv) a second electrode in said trench, said second electrode in said broad lower region comprising a first layer of polysilicon over said node dielectric, a refractory metal salicide layer over said first polysilicon layer and a second polysilicon layer over said salicide.

8. The capacitor structure of Claim 7 comprising a collar oxide about said narrow upper trench region.

9. A memory cell device comprising the trench capacitor structure of Claim 7 or Claim 8.

10. A capacitor structure in a semiconductor substrate, said capacitor structure comprising (i) a trench having a upper region and a lower region, (ii) an electrode in said substrate about said lower region, (iii) a conformal node dielectric lining said trench at said electrode, and (iv) a second electrode in said trench, said second electrode in said lower region comprising a first layer of polysilicon over said node dielectric, a refractory metal salicide layer over said first polysilicon layer and a second polysilicon layer over said salicide.

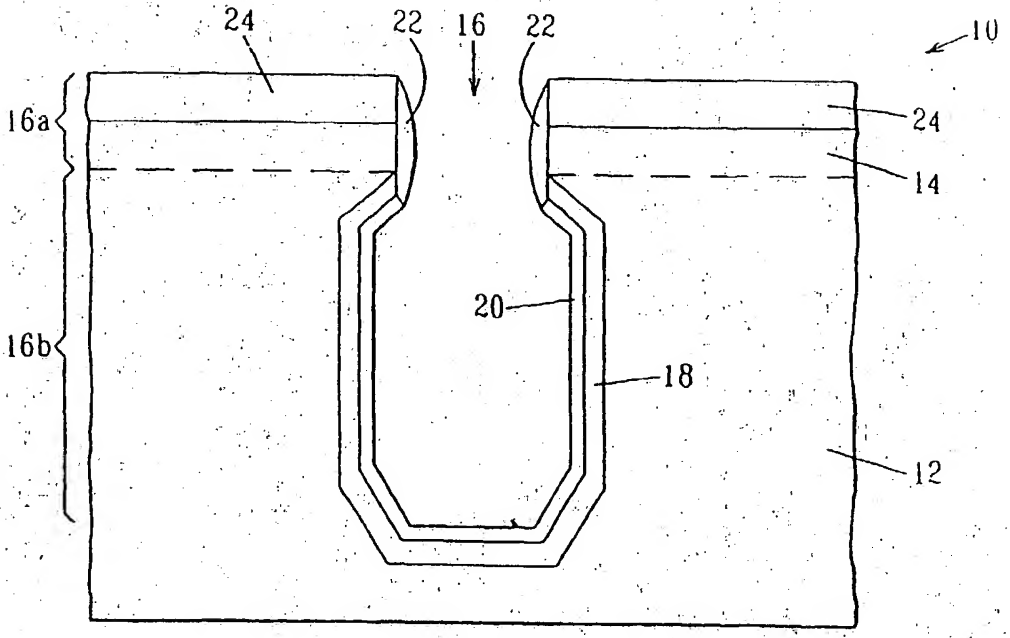
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FIG. 1(a)

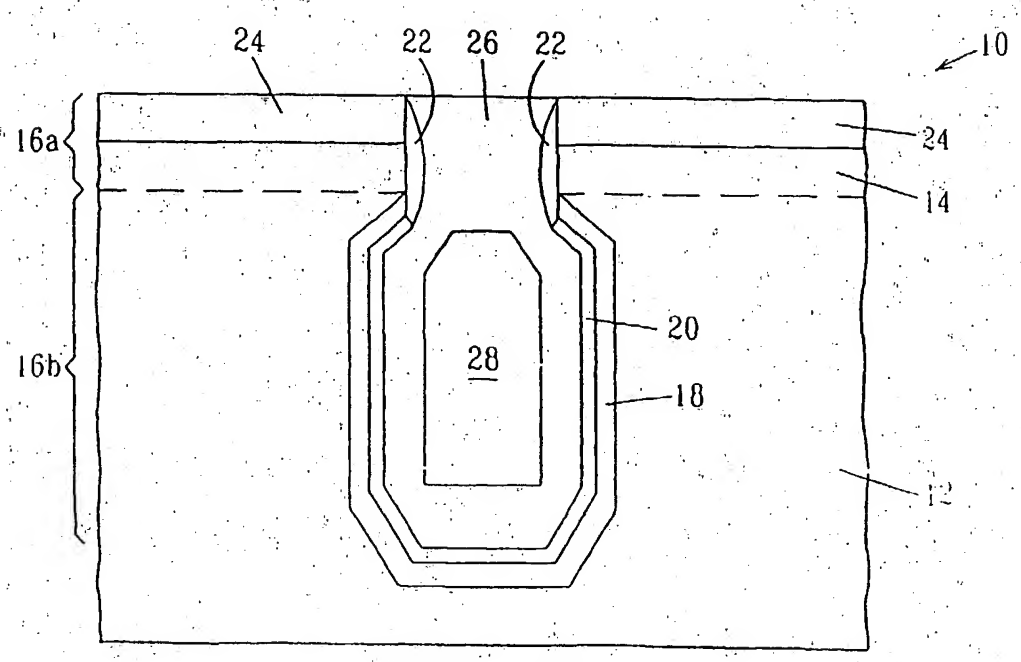
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FIG. 1(b)

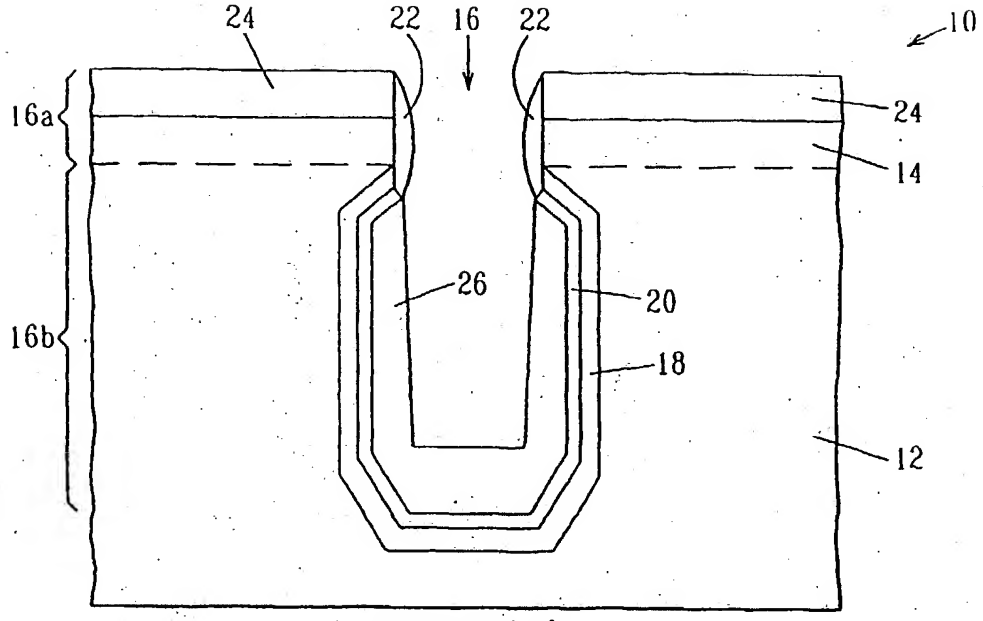
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FIG. 1(c)

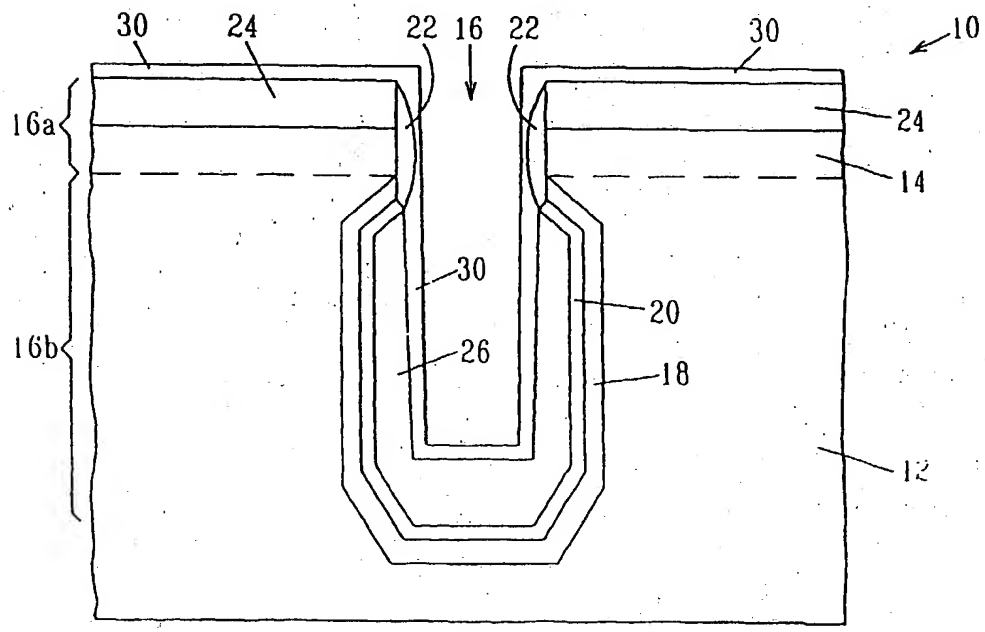
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FIG. 1(d)

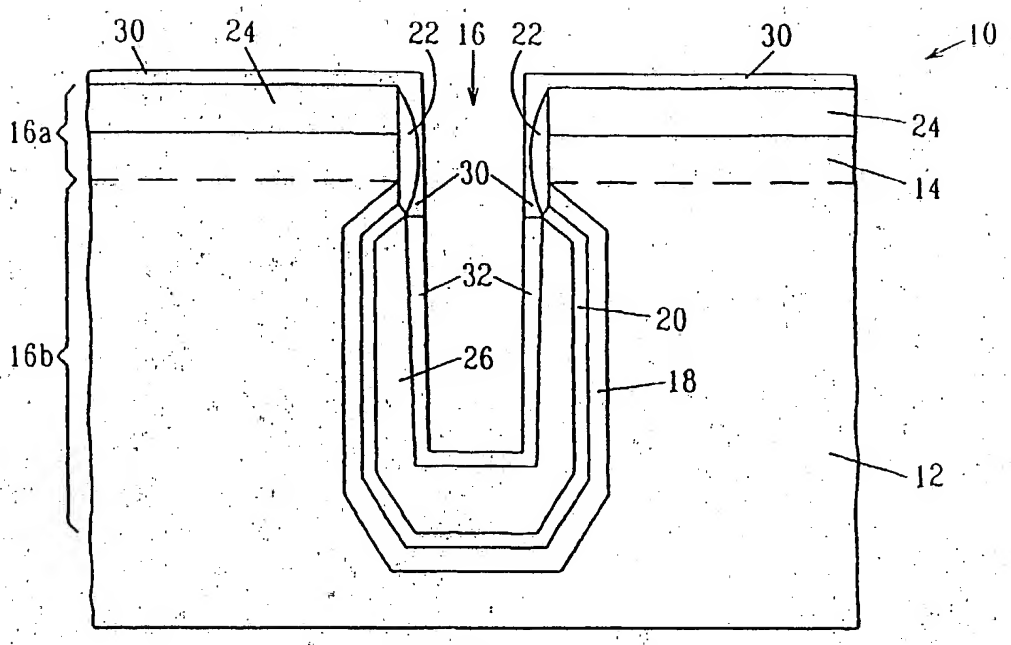
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FIG.1(e)

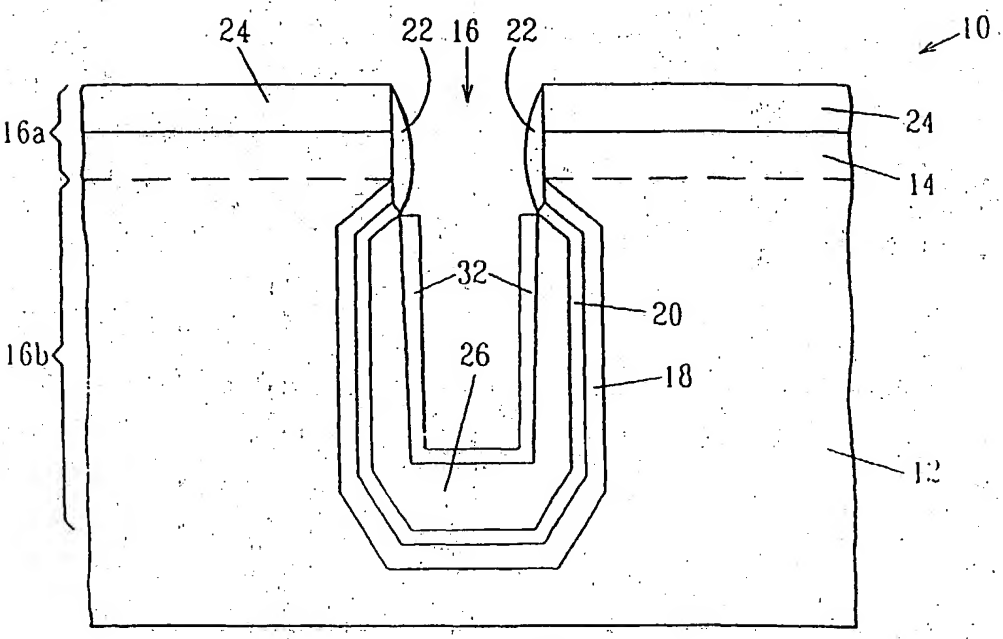
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FIG.1(f)

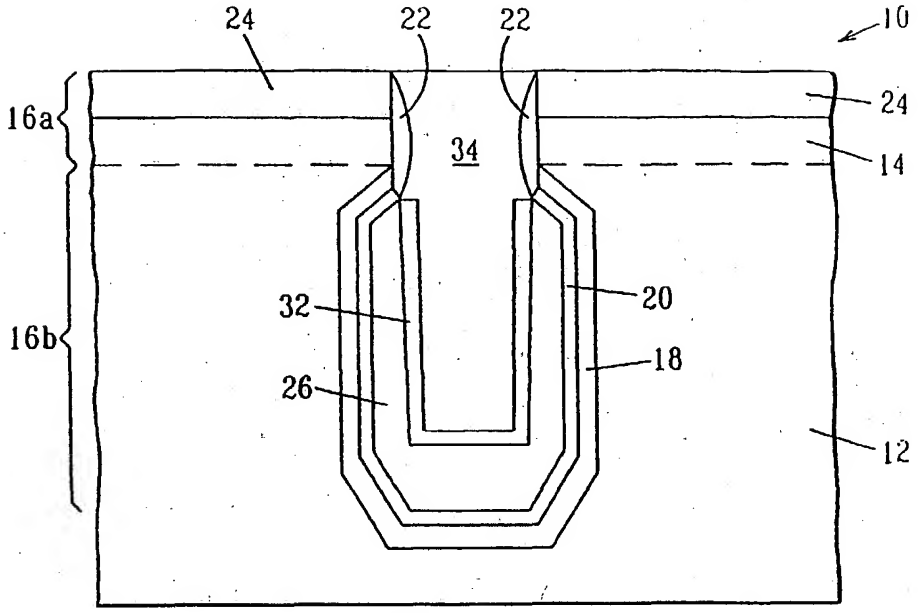

FIG.1(g)

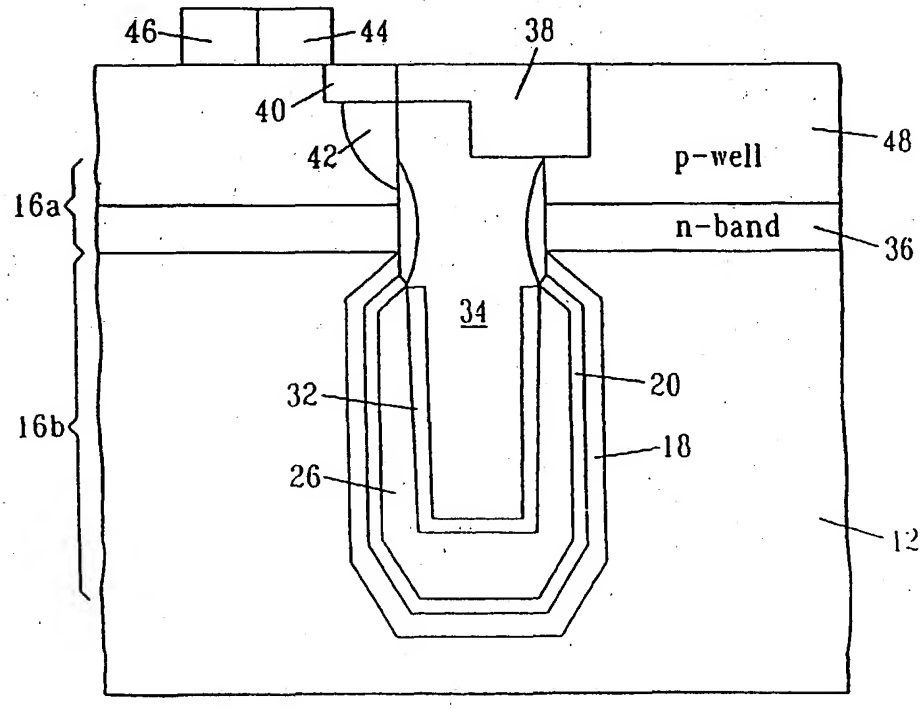

FIG.2

Docket # 28P-INF-N10309
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